## USB Feature

### Block Diagram



Fig.1.1 USB block diagram

### General Features

* Same programming model for SuperSpeed (SS), High-Speed (HS), Full-Speed (FS), and  
  Low-Speed (LS)
* 150Mhz 32-bit slave interface for CSR and RAM Debug access
* 150Mhz 64-bit master interface for internal DMA access
* Independent Little or Big Endian (byte invariant) mode selection for both Slave and Master interface
* Independent Endian selection between descriptor and data fetch
* Hardware/software race condition avoidance in systems with bridge
* Concurrent read and write operations to get the best performance of USB 3.0 duplex operation in AXI bus mode
* AHB Slave interface:
* Supports all AHB Burst types, including WRAP# supports
* Does not generate Split, Retry, or Error responses
* AXI Master interface:
* The software can select the allowable burst lengths (single, burst 4/8/16/32/64/128/ 256 as pplicable) by programming the GSBUSCFG0 register in CSR
* Handles fixed burst address alignment. Starting address of an burst is always aligned to burstsize; even though AXI specification does not require this, most memory/cache access require this. For example, if a burst of 8 is selected in a 64-bit wide data bus, the burst starting address will be 0, 64, 128, etc
* Software can select the number of outstanding read/write requests (1 to 16) made by the AXI Master Interface by programming the GSBUSCFG1 register in CSR. Read and write channels operate independently and may each have their own outstanding requests limited by the programmed value in GSBUSCFG1
* Capable of performing zero-wait state data transfers
* Handles the AXI 4k boundary, Transfers are split to prevent crossing of the 4k boundary. Optionally, handles break up transfers on the 1k boundary by utilizing a software programmable option in the GSBUSCFG1 in the CSR
* Supports cacheable accesses on the AXI Master Interface
* Does not support Atomic and Protected accesses on AXI Master

### USB 3.0 Device Features

* Up to 8 bidirectional endpoints, including control endpoint 0
* Software directly handles non-timing-critical and rarely occurring tasks, such as control transactions
* Flexible endpoint configuration allows a single area optimized configuration meeting multiple applications, software can map the USB endpoint to an endpoint resource number, even if the USB endpoint numbers are not contiguous.
* Dynamic mappable TxFIFOs to support more Tx-endpoints than the physical FIFOs
* Simultaneous IN and OUT transfer support
* 4 Gbps IN and 4 Gbps OUT bandwidth (interpacket delays and protocol overhead included)
* Descriptor caching and data pre-fetching for predictable performance in high-latency systems
* Hardware handles ERDY and burst
* Hardware handles all data transfers Capability to set up multiple transfers without interrupting the host processor on every transfer
* Stream-based bulk endpoints with controller automatically initiating data movement
* Isochronous endpoints with isochronous data in data buffers or external hardware FIFOs
* Flexible Descriptor with rich set of features to support buffer interrupt moderation, multiple transfers, isochronous, control, and scattered buffering support

### USB 3.0 xHCI Host Features

* Up to 64 devices
* xHCI1.0 compatible
* Standard or open-source xHCI and class drivers
* xHCI features:
* Aggressive power management
* Clean software and hardware interface
* Memory access optimization
* Interrupt Moderation
* Descriptor caching for predictable performance in high latency systems
* Concurrent IN and OUT transfers to get the full 8 Gbps duplex throughput (interpacket delays and protocol overhead included)
* Concurrent USB 3.0/2.0/1.1 traffic:
* Designed so that USB 2.0 Devices do not degrade the overall throughput
* Net bandwidth increased to 8.48 Gbps (8 Gbps USB 3.0 bandwidth plus 480 Mbps USB 2.0 bandwidth)
* Dual power rail designs with hibernation feature